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TAS5632

250-W Stereo PurePath[™] HD Digital Input High Efficiency Power Stage

Check for Samples: TAS5632

FEATURES

- PurePath[™] HD Integrated Feedback Provides:
 - 0.025% THD at 1 W into 4 Ω
 - >65 dB PSRR (No Input Signal)
 - >105 dB (A weighted) SNR
- Pre-Clipping Output for Control of a Class-G Power Supply
- Reduced Heat Sink Size due to use of 120mΩ Output MOSFET with
 - >90% Efficiency at Full Output Power
 - >81% Efficiency at 1/8 Output Power
- Output Power at 10%THD+N
 - 250 W / 6 Ω BTL Stereo Configuration
 - 190 W / 8 Ω BTL Stereo Configuration
- Output Power at 1%THD+N
 - 200 W / 6 Ω BTL Stereo Configuration
 - 150 W / 8 Ω BTL Stereo Configuration
- Click and Pop Free Startup
- Error Reporting Self-protected Design with UVP, Over Temperature, and Short Circuit Protection
- EMI Compliant when used with Recommended System Design
- 48-Pin SSOP (DKQ) Package for Reduced Board Size

APPLICATIONS

- Blu-ray™/DVD Receivers
- Mini Combo Systems
- AVR Receivers
- Powered Subwoofer and Active Speakers

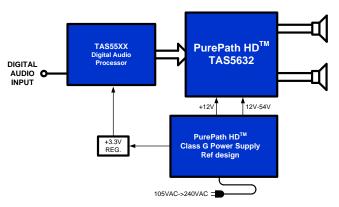
DESCRIPTION

The TAS5632 is a high power version of the high efficient class-D power amplifier TAS5624 with increased nominal supply voltage of 54V. Using large MOSFETs and a novel gate drive scheme for high power efficiency and reduced power loss in idle and at low output effectively reduces heat sink size requirements.

The unique pre clipping output signal can be used to control a Class-G power supply, this combined with the low idle loss and high power efficiency of the TAS5632 leads to industry leading levels of efficiency ensuring a super "green" system.

The TAS5632 uses constant voltage gain. The internally matched gain resistors ensure a high Power Supply Rejection Ratio giving an output voltage only dependent on the audio input voltage and free from any power supply artefacts.

The high integration of the TAS5632 makes the amplifier very easy to use and using TI's reference schematics and PCB layouts leads to fast design in time. The TAS5632 is available in the space saving surface mount 48-pin SSOP package.



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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
TAS5632DKQ	PREVIEW	HSSOP	DKQ	48	25	TBD	Call TI	Call TI			
TAS5632DKQR	PREVIEW	HSSOP	DKQ	48	2000	TBD	Call TI	Call TI			

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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